

Low Noise, High PSRR, Replica LDO

1.Features

Power Supplies : 1.2 V, 1.8 V
 Output voltage : 0.8 V
 Quiescent current: 7.3 mA
 Maximum current: 74.8 mA
 Reference Voltage: 0.8 V
 PSRR ⁽¹⁾: 70 dB @1 KHz, 1.8 V
 65 dB @1 KHz, 1.2 V
 PSRR ⁽¹⁾: 48 dB @1 MHz, 1.8 V
 20 dB @1 MHz, 1.2 V
 Noise @1KHz: -145 dBV/sqrt (Hz)
 (53 nV/sqrt (Hz))
 Noise @1MHz: -174 dBV/sqrt (Hz)
 (1.9 nV/sqrt (Hz))
 Bandwidth: 6.86 KHz
 Drop-out voltage: 3.8 uV (vdd12 : 1 V – 1.2 V)
 Load regulation:
 -3.6 mV/mA Iload from 0-60mA
 (-2.6 mV/mA Iload close to 20mA)
 WakeUp Time : 11 ns
 Area : 280 um x 170 um
 Process : 22FDX
 Metal Option : 19

(1)Filter: R=10Kohm, C=81pF

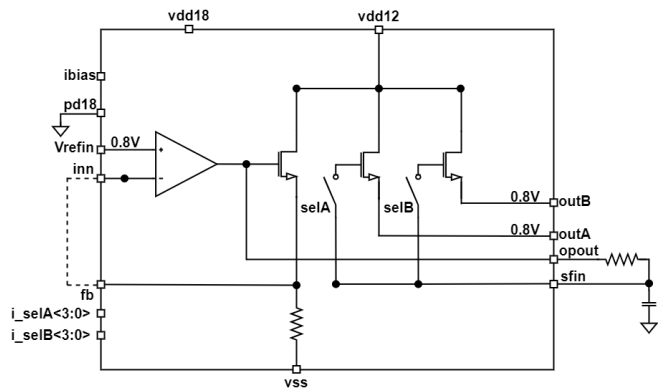
2.Applications

VCOs, PLLs, Power Supply Noise sensitive circuits. Circuits with low line regulation requirements

3.Description

The WEALDORP1812NI08SFN22M22G is a voltage regulator operating from 1.8 V and 1.2 V powersupplies. The WEALDORP1812NI08SFN22M22G provides two 0.8 V outputs. The outA output has double current driving capability compared to outB. Due to poor dc-line regulation the accuracy of the output voltage can be calibrated through a 4 bit binary control when the load current varies under a wide range.

Simplified Schematic



4. PinOut Description

Pinout	Purpose ⁽¹⁾	Description
vdd12	PS	1.2 V Input Supply Voltage
vdd18	PS	1.8 V Input Supply Voltage
vss	GND	Power Ground
ibias	AIO	25uA Bias Supply
pd18	DI	Power Down pin. Drive pd18 to vss to turn on the regulator. Drive pd18 to vdd18 to put the voltage regulator (LDO) into power down mode.
Vrefin	I	0.8 V Reference Voltage
inn	I	Negative Opamp Input
fb	IO	Feedback
i_selA<3:0>	I	iLoad control bits for outA
i_selB<3:0>	I	iLoad control bits for outB
selA	I	Selects the outA
selB	I	Selects the outB
opout	IO	Operational Amplifier output for filtering
sfin	IO	LDO device nfet gate
outA	O	0.8 Output Voltage
outB	O	0.8 Output Voltage

5. iLoad control bits

i_selA<3:0>	iLoad(mA)	i_selB<3:0>	iLoad(mA)
0000	0	0000	0.0
0001	3	0001	1.5
0010	6	0010	3.0
0011	9	0011	4.5
0100	12	0100	6.0
0101	15	0101	7.5
0110	18	0110	9.0
0111	21	0111	10.5
1000	24	1000	12.0
1001	27	1001	13.5
1010	30	1010	15.0
1011	33	1011	16.5
1100	36	1100	18.0
1101	39	1101	19.5
1110	42	1110	21.0
1111	45	1111	22.5

(1) I=Input, O=Output, IO=Input,Output ,PS=Power Supply, DI= Digital Input, AIO=Analog Input Output

Availability

GF 22FDX, Metal Option 19





Deliverables

GDSII, Database, SystemVerilog Models

About weasic

Weasic Microelectronics S.A. designs, develops, and markets high quality complex analog and RF IP for the wired and the wireless communications industries, helping semiconductor and system companies to shrink the product design cycle. Weasic, silicon verified, IP is designed in the state-of-the-art CMOS and SiGe processes and can be easily ported and customized to serve the development of transceivers for 5G communications, Mobile Backhaul, RADAR sensors and 802.11.* applications.

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