Direct Digital Synthesis

1. Features

Area : 30 um x 16 um
Process : 22FDX
Metal Option : 19

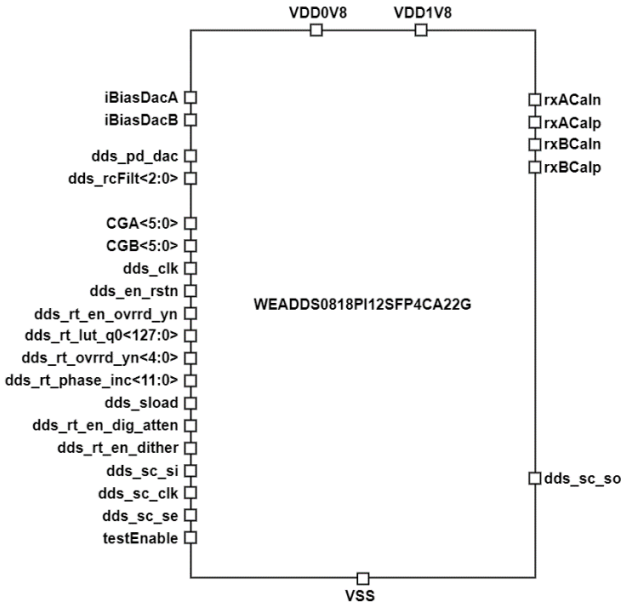
2. Applications

VCOs, PLLs, Power Supply Noise sensitive circuits. Circuits with low line regulation requirements

3. Description

The WEADDS0818PI12SFP4CA22G block generates a sine(x) (or any other odd periodic function) analog signal, to be used for calibration purposes. The block consists of the digital Numerically Controlled Oscillator (NCO), followed by a Digital to Analog Converter (DAC). The NCO is clocked at 425 MHz and its output is a 5-bit symbol of the sine(x) waveform.The NCO has a runtime configuration of the desired output waveform, in fact it takes only the first quarter (compressed) Look-Up-Table and generates the whole period by flipping and mirroring it. The frequency is also runtime configurable by a phase increment variable and the gain is mainly configurable by an analog control, although there is the provision of a digital div-by-2 attenuator.

Simplified Schematic



4. Pin Out Description

Pinout	Purpose	Description
VDD0V8	PS	0.8 V Input Supply Voltage
VDD1V8	PS	1.8 V Input Supply Voltage
VSS	GND	Ground
iBiasDacA	AIO	25uA Bias Supply
iBiasDacB	AIO	25uA Bias Supply
dds_pd_dac	DI	
dds_rcFilt<2:0>	I	Programmable Capacitor load at the current output Minimum: 10pF Maximum : 80pF
dds_agcA<5:0>	I	Programmable Current Minimum multiply X 1 , Maximum multiply X 64
dds_agcB<5:0>	I	Programmable Current Minimum multiply X 1 , Maximum multiply X 64
dds_clk	DI	Module's functional Clock, connected to a 425 MHz source.
dds_en_rstn	DI	Asynchronous Reset (Active Low). It is synchronized, inside the current module, with clk, before use. In Test Mode, reset synchronizer is made transparent and reset is directly controllable by the Tester via the dds_en_rstn input.
dds_rt_en_ovrrd_yn	DI	Enable Override (Debug Tie-off) Output Symbol. When this signal is 1, or dds_load is 1, the output symbol is updated by the value of dds_rt_ovrrd_yn at every cycle.
dds_rt_lut_q0<127:0>	DI	Runtime LUT Samples (Quarter-0 of the sine(x) function). 32 samples 4 bits per sample. The recommended value to generate a full swing sine(x) function is the 0xfffffeeeedddccbbaa98876654432110.
dds_rt_ovrrd_yn<4:0>	DI	Override (Debug Tie-off) Output Symbol Value (when rt_en_ovrrd_yn==1)
dds_rt_phase_inc<11:0>	DI	12-bit Phase Increment, in [0, 4095]. The Reset Value 0x060 generates a 10 MHz sine(x) given that dds_clk is @425 MHz.
dds_sload	DI	Synchronous Clear/Load (Active High) & Enable (Active Low) at the same time. It is synchronized, inside the current module, with dds_clk, before use.

		To avoid glitches being caught by the synchronizer, ensure this signal is registered externally. When this signal is 1, or dds_rt_en_ovrrd_yn is 1, the output symbol is updated by the value of dds_rt_ovrrd_yn at every cycle.
dds_rt_en_dig_atten	DI	Digital Attenuator Enable. When 1, output Symbol is Digitally Divided by 2.
dds_rt_en_dither	DI	Enable Dithering. Recommended value is 1 for best results.
dds_sc_si	TEST-DI	Test Mode Scan In-1.
dds_sc_clk	TEST-DI	Test Mode Clock.
dds_sc_se	TEST-DI	Test Mode Scan Enable, Active High.
testEnable	TEST-DI	Test Mode Enable, Active High. Controlled by the Tester, usually activated throughout the testing. Tie-off to 0 during normal operation.
rxACaln	O	Positive Current output A (10uA – 1.5mA)
rxACalp	O	Negative Current output A (10uA – 1.5mA)
rxBCaln	O	Positive Current output B (10uA – 1.5mA)
rxBCalp	O	Negative Current output B (10uA – 1.5mA)
dds_sc_so	TEST-DO	Test Mode Scan Data Out-1.

(1) I=Input, O=Output, IO=Inpout,Output ,PS=Power Supply, DI= Digital Input,DO=Digital Output, AIO=Analog Input Output

5. Availability

GF 22FDX, Metal Option 19

6. Deliverables

GDSII, Database, SystemVerilog Models

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