

## Passive Programmable High Pass Filter

### 1. Features

Power Supply : 1.8 V  
 Cutoff frequency : 2 MHz to 27.5 MHz  
 Max Gain : 0 dB  
 Programmable gain  
 Consumption : 0 mW  
 Area : 564  $\mu\text{m}$  x 133  $\mu\text{m}$   
 Process : 22FDX  
 Metal Option : 19

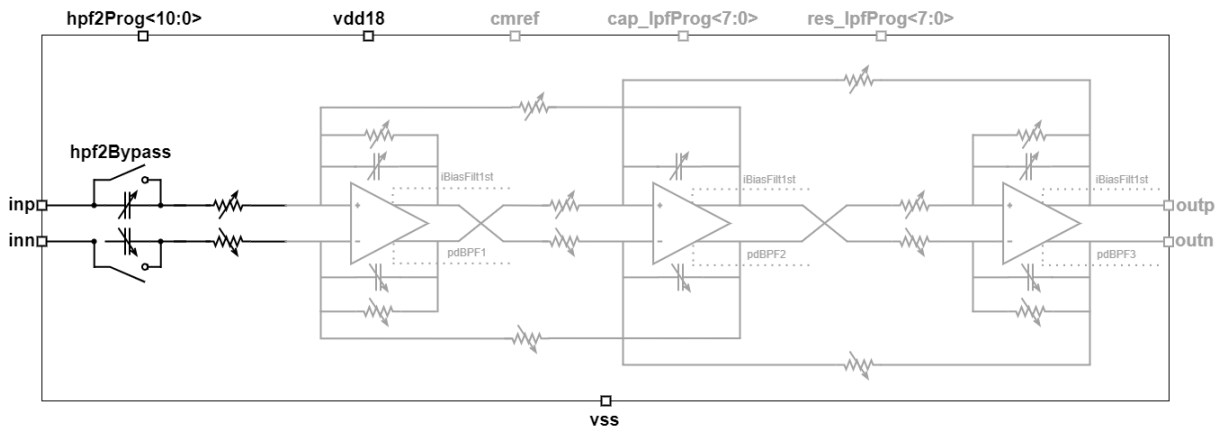
### 3. Description

The WEA228HPFP18BT122G is a passive High Pass filter with programmable cutoff frequency from 2 MHz to 27.5 MHz with less than 10.5 % residual absolute error after calibration. The filter supports capacitor bypass mode.

### 2. Applications

Receivers, RADAR

### Simplified Schematic



## 4. Pin Out Description

Pinout	Purpose	Description
vdd18	PS	1.8 V Input Supply Voltage
vss	GND	Power Ground
inp	I	Positive Input
inn	I	Negative Input
pdBPF2	DI	Power Down pin. Drive pd18 to vss to turn on the OpAmp. Drive pd18 to vdd18 to put the Opamp into shutdown mode.
hpf2Prog<10:0>	DI	High Pass cutoff programming
hpf2Bypass	DI	High Pass Filter Bypass

(1) I=Input, O=Output, IO=Input,Output ,PS=Power Supply, DI= Digital Input, AIO=Analog Input Output

## 5. HPF Cutoff Frequency Programming Table

Hpf2Prog<10:0>=hpf2Prog\_bin<2:0> hpf2Prog\_thermo<7:0>

(MHz)	00000000	00000001	00000010	00000100	00001000	00010000	00100000	01000000	10000000
<b>000</b>	27.08	7.29	4.24	3.00	2.32	1.89	1.60	1.39	1.22
<b>001</b>	20.08	6.69	4.03	2.89	2.25	1.85	1.57	1.36	1.21
<b>010</b>	16.00	6.18	3.84	2.79	2.20	1.81	1.54	1.34	1.19
<b>011</b>	13.32	5.74	3.67	2.70	2.14	1.77	1.51	1.32	1.17
<b>100</b>	11.42	5.36	3.51	2.61	2.08	1.73	1.49	1.30	1.16
<b>101</b>	9.99	5.03	3.37	2.53	2.03	1.70	1.46	1.28	1.14
<b>110</b>	8.90	4.74	3.23	2.46	1.98	1.66	1.43	1.26	1.13
<b>111</b>	8.01	4.48	3.11	2.39	1.94	1.63	1.41	1.24	1.11

## 6. Availability

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GF 22FDX, Metal Option 19

## 7. Deliverables

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GDSII, Database, SystemVerilog Models

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## About weasic





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**weasic Microelectronics S.A.** designs, develops, and markets high quality complex analog and RF IP for the wired and the wireless communications industries, helping semiconductor and system companies to shrink the product design cycle. Weasic, silicon verified, IP is designed in the state-of-the-art CMOS and SiGe processes and can be easily ported and customized to serve the development of transceivers for 5G communications, Mobile Backhaul, RADAR sensors and 802.11.\* applications.

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## Contact us

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