WEA20SFMCWI22G

19 GHz to 20.25 GHz FMCW Modulator for RADAR

1 Features

QFN48 7mm X 7mm
Power Dissipation: 480mW
Output power: 10 dBm
Reference input: 20 MHz to 100 MHz
Output frequency range: 19 GHz to 20.25GHz
Low PN (SSB): -103 dBc/Hz at Δf=1MHz Excellent linearity: < 0.2%
Maximum chirp modulation BW: 2.15 GHz[1]
Chirp up / retrace slopes: 100 / 2000 MHz/us[1,2]
Lock time: < 10us
Programmable Chirp Profiles
Programmable Loop Filter
Bank of LC-VCOs with 128 Bands/VCO
Automatic VCO/Band Selection System
50% duty cycle Linear Chirp modulation with interleaved PLL operation
Analog Test Bus functionality for real-time FuSa functionality

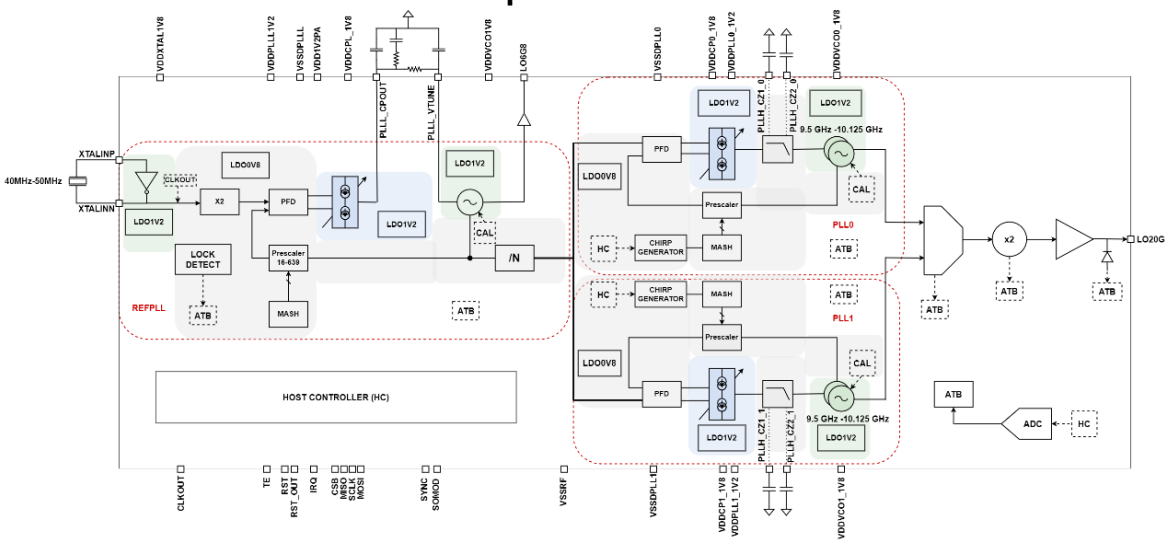
2 Applications

FMCW RADAR applications (automotive)

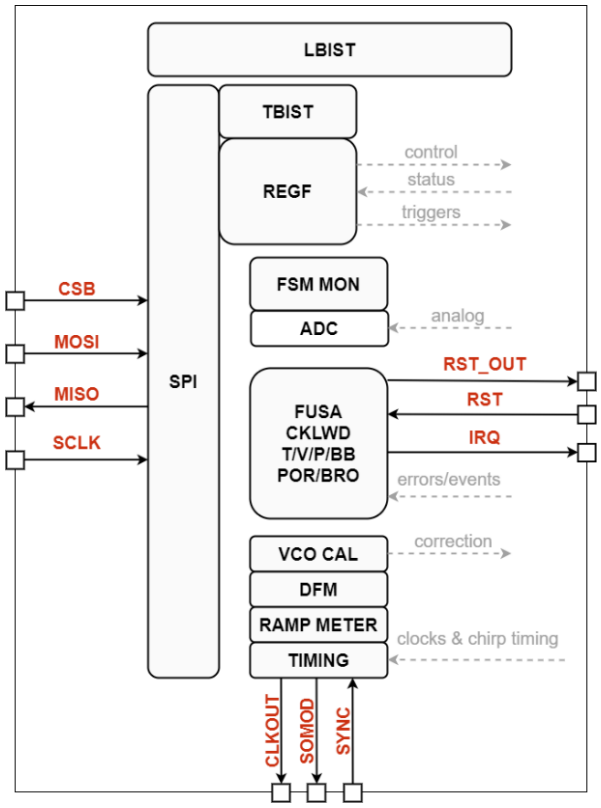
3 Description

The WEA20SFMCWI22G is an ultra-linear FMCW modulator consisting of 3 integrated PLLs. One PLL provides a high frequency Reference signal and the other two are performing the chirping function. The dual chirping PLL can be used either as i) 50% interleaved mode, or ii) coherent in-phase operation with a +3dB Phase Noise improvement for LRR mode. The synthesizer uses a reference input ranging from 20 MHz to 100 MHz, and can operate from either an external signal source or with a single external Crystal Oscillator. The modulator has a phase synchronization capability for coherent operation with other modulators. It also provides synchronized trigger event signals for the RADAR Transmitter and Receiver chips. By the use of internal high PSRR LDOs, the WEA20SFMCWI22G can withstand the noisy supply environment. It is powered by 1.2 V and 1.8 V supplies.

Simplified Schematic



[1] Referenced at 80GHz
[2] Retrace slope in interleaved PLL mode

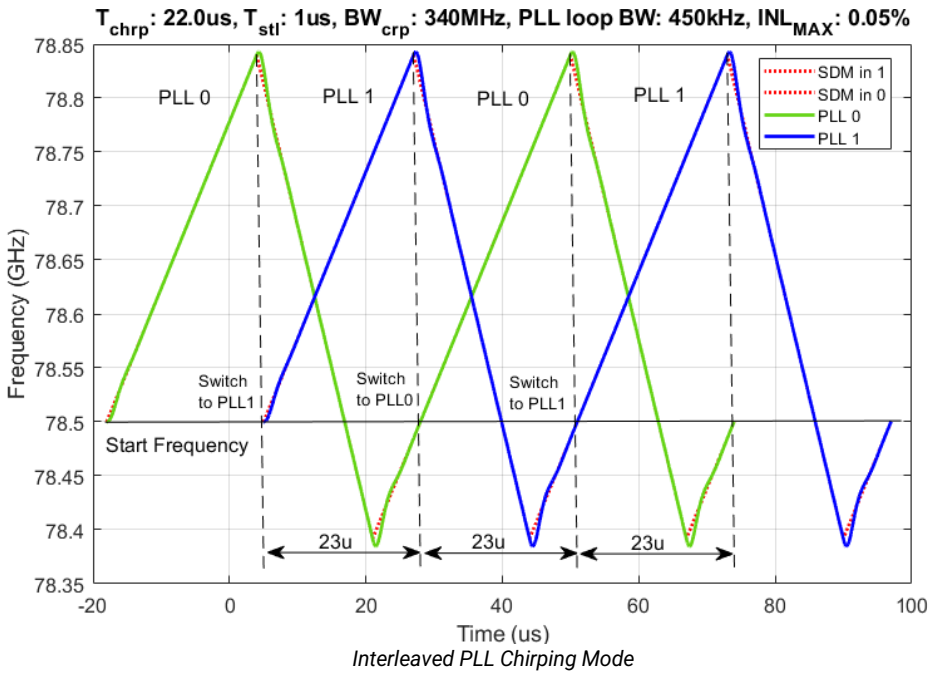


Functional Block Diagram of the Controller

SPI: SPI Interface, for Control & Status by the system Host
REGF: SPI Register File, stores chip configuration
TBIST: Transparent BIST of Reg file contents, checks for SEUs (Single-Event-Upsets). Periodically triggered by a timer, verifies the CRC of the **REGF** registers, serially bit by bit
LBIST: Logic BIST of the whole chip. Checks for stuck-at faults, by applying test vectors into the scan chains
FUSA: Functional Safety Features (on chip):

- **T/V/P** Temperature / Voltage / Power (over/under)
- **POR/BRO**: Power-On-Reset, Brown-Out-Detector.
- **CLKWD**: Clock Watchdog, issues an error flag when clock stops toggling
- **FSM_MON**: Continuous Monitor, periodically triggered by a timer, measures sensors by the ADC and issues error flags when out of certain thresholds
- **DFM**: Digital Frequency Meter. Measures the clock frequency of the one clock, using the other clock as reference
- **RAMP_METER**: Measures the Ramp Frequency during chirping and issues error flags when out of certain thresholds
- **BALL_BREAK_DETECTOR**: Detects whether the connection to the RF circuit is broken or not
- **PLL_LOCK_DETECTOR:** Detects whether the PLL is locked or not
- **SPI_CRC:** CRC code for the SPI messages
- **ERROR_PIN:** Separate error notification pin

VCO_CAL: Auto-Calibration algorithms of the chip VCOs. Tune VCO capacitors and eliminate frequency drift due to manufacturing process variations



Interleaved PLL Chirping Mode

4. Availability

GF 22FDX, Metal Option 19

5. Deliverables

GDSII, Database, SystemVerilog Models

About weasic

Weasic Microelectronics S.A. designs, develops, and markets high quality complex analog and RF IP for the wired and the wireless communications industries, helping semiconductor and system companies to shrink the product design cycle. Weasic, silicon verified, IP is designed in the state-of-the-art CMOS and SiGe processes and can be easily ported and customized to serve the development of transceivers for 5G communications, Mobile Backhaul, RADAR sensors and 802.11.* applications.

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