WEA7681TX22G

76 GHz to 81 GHz FMCW Radar Transmitter

1. Features

Output Frequency Range: 76 GHz to 81 GHz
Input Frequency Range: 19 GHz to 20.25 GHz
Power Supply Voltages: 1.8 V Analog, 0.8 V Logic, 1.25 V to 1.6 V Power Amplifier
Power at BGA output: 17 dBm (Includes 1.6dB loss from package to silicon transition)
2x8 Bit Binary Controlled Cartesian Phase Shifter with Range 0 - 360° and 2.8° degrees of accuracy
Turn ON/OFF time: < 100 ps
Automotive Grade 1 (-40 °C to 125 °C)
Power Consumption: 947 mW
Area:1500 um x 460 um

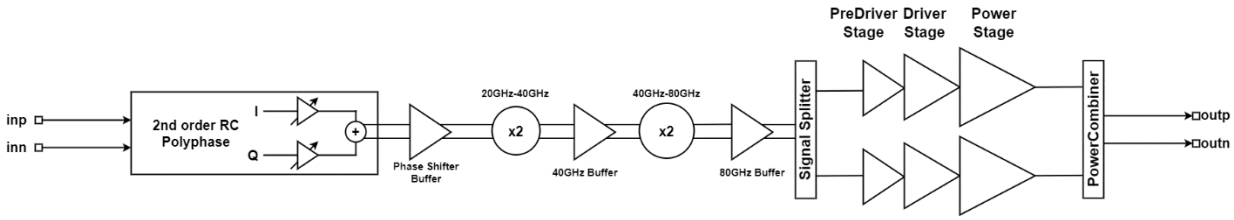
3. Description

The WEA7681TX22G is a transmitter chain for radar applications covering the 76 GHz to 81 GHz automotive band. The transmitter chain consists of a programmable phase shifter, two frequency doubler stages and a 3-stage power amplifier. All the stages are supported by programmable bias current circuitry. The transmitter has a dual power detector scheme for optimum transmit power management and has a build-in Analog Test Bus (ATB) for complete monitoring of the bias condition of all whole IP for FUSA. It is implemented in 22FDX FD-SOI process. The WEA7681TX22G occupies a silicon area of 1500 um x 460 um.

2. Applications

Radar applications

Simplified Schematic



4. Transmitter Performance

Parameter		Test Conditions	Min	Typ	Max	Unit
TX Slice						
Input frequency Range			19.0		20.25	GHz
Output Frequency Range			76.0		81.0	GHz
Output Power		Normal mode(1). Including the losses of package to silicon transition	13.4	17	17.9	dBm
		LP1 mode(2). Including the losses of package to silicon transition	5.62	14.5	15	dBm
		LP2 mode(3). Including the losses of package to silicon transition	3.35	12	12	dBm
		variation over chirp BW (1GHz)	-1.4		-0.07	dB
Power Consumption		Normal mode (1)		947	1418	mW
		LP1 mode(2)	497	650	667	mW
		LP2 mode(3)	412	486	542	mW
		Power Down mode : Fast – off (4)	8.87	10.5	13.5	mW
		Power Down mode : Slow - off (5)	3.58	4.79	7.2	mW
Power Variation over temperature		normal mode – Over temperature range : -40 -125 with 55ºC step.	0.07		0.93	dB
Minimum output power capability – TPC (6)		VDDPA=1V	-34	0		dBm
Settling Time		From stand by to compression		4.9		ns
Phase Noise	@1MHz	From Rx/Tx split point to PA output. The uncorrelated noise portion. Referred to 80GHz	-121.5	-131.6	-133.0	dBc/Hz
	@ 10MHz		-125.7	-138.5	-139.9	dBc/Hz
	@ 45MHz		-133.4	-141.4	-142.8	dBc/Hz
	> 45MHz		-135.7	-142.2	145.2	dBc/Hz
Output Return Loss		Measured at BGA with 50 Ohm Load and 10 dB VSWR	-38.9	-17.2	-8.47	dB
Output Power (PA off)		PA-Fast off (4)	-41	-37.2	-30.9	dBm
		PA-Slow off (5)	-40.3	-38.2	-34.6	dBm
Phase step - Size and Accuracy (=Error window)		Referred to ideal grid	1.43	2.81	4.2	deg
Phase range			0		360	deg
Phase settling time to error-window accuracy		100MHz switching time			0.2	nsec
Tx output power change due to phase-shift			0.08		0.16	dB

(1) VDDPA:1.6 V, (2) VDDPA=1.35V, (3) VDDPA=1.25V, (4) Standby mode. Bias circuits are operating, RF blocks are powered down, (5) Bias circuits and RF blocks are powered down, (6) Transmitter Power Control

Parameter	Test Conditions	Min	Typ	Max	Unit
VDDLO	0.8 V +/– 5%	155	228	297	mA
		118	182.4	250	mW
VDDAUX	1.8 V +/– 5%	20.3	24.7	30.4	mA
		34.7	44.46	57.5	mW
VDDPA	1.6 V +/– 5%	239	353	630	mA
		363	565	1058	mW

5. Block Description

5.1 TX Slice

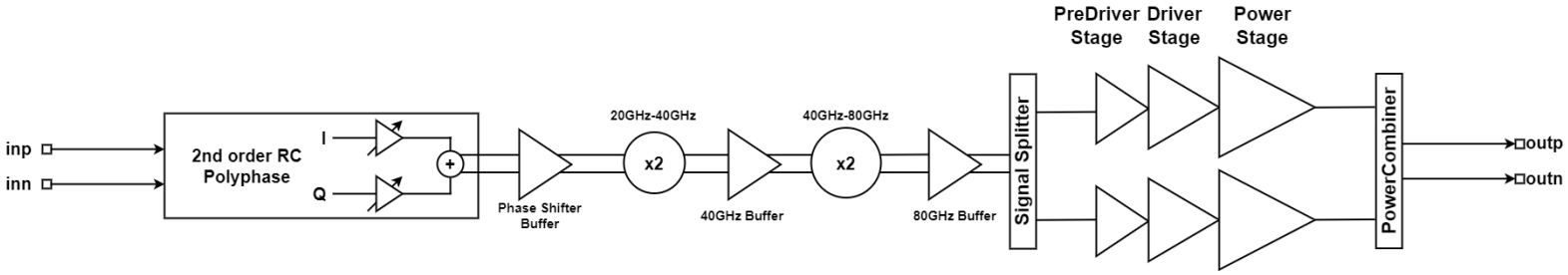
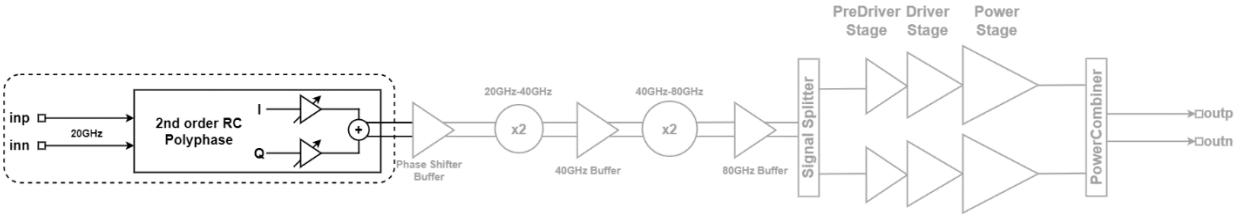


Figure 1. Tx Slice Simplified Schematic

5.2 TX LO Phase Shifter



The phase shifter performs 0 - 90 degrees phase shift enabling the use of the transmitter in phased array RADAR systems. The input of the block is a differential signal at a frequency range of 19GHz to 20.25GHz. After the signal frequency quadrupling from the subsequent stages the phase shift is 0º-360º. To set a specific signal phase shift the GainI and GainQ should be programmed using the control signals phaseSelI<6:0> and phaseSelQ<6:0> respectively, according to the following equation:

$$GainI = Round\left(127\ Sin\left(\frac{\pi\ \varphi}{180}\right)\right)$$

$$GainQ = Round\left(127\ Cos\left(\frac{\pi\ \varphi}{180}\right)\right)$$

where φ is the desired phase shift.

The phase shifter is powered through 1.8V supply.

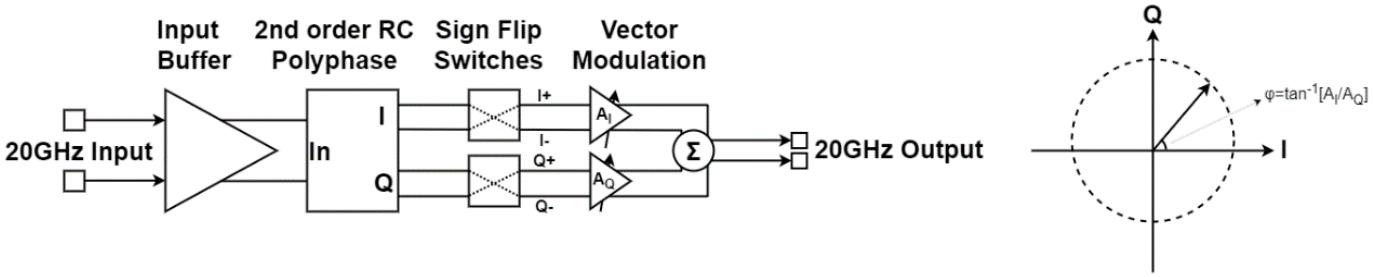


Figure 2. Tx LO Phase Shifter Simplified Schematic

Phase shift	Gain I	Gain Q
0	0	127
15	33	123
30	64	110
45	90	90
60	110	64
75	123	33
90	127	1

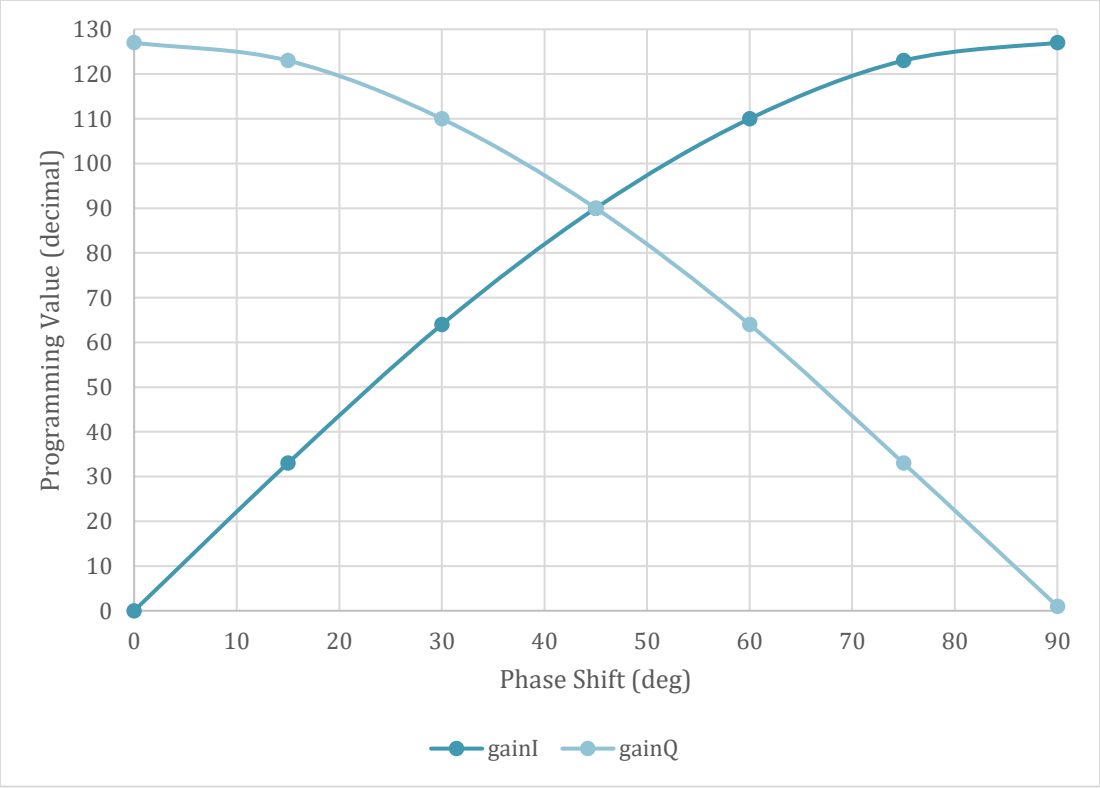


Figure 3. Indicative nominal programming of the 2nd order RC Polyphase Filter gain

5.3 TX Slice Frequency Multiplier

The TX LO Frequency Multiplier circuit consists of two frequency doubler stages. Each doubler is driven by an amplifier stage to maintain high input swing and subsequently high up-conversion gain. The last buffer stage drives the first stage of the power amplifier via an integrated transformer. The bias conditions of all the blocks are digitally programmable. All the frequency multiplier stages are powered through a 0.8V supply.

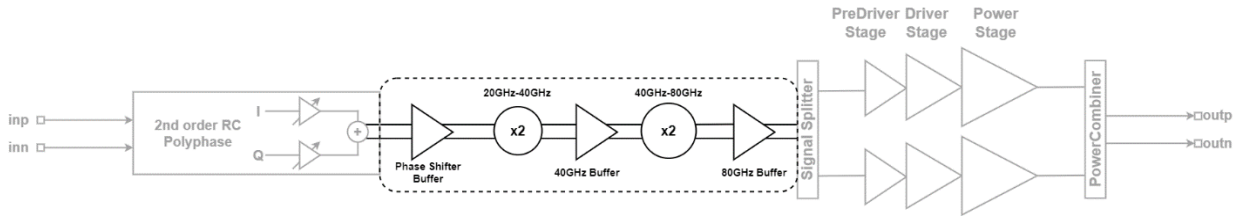


Figure 5. TX Frequency Multiplier Simplified Schematic

5.7 TX Power Amplifier

The Power Amplifier consists of two parallel three stage amplifiers, a splitter at the input and a combiner at the output. The power cells are differential cascode amplifiers. The architecture utilizes power combining at the output to increase the output power.

The transformer-based combiner also acts as a differential to single ended balun. At the input and output nodes there is a power sensor. The output power sensor is used to calibrate the bias of the driving stage to ensure reliability and adequate signal level over process variation. The power amplifier system supports three modes of operation, normal mode, low power mode 1, and low power mode 2. Normal mode uses 1.6 V supply and outputs the higher power with maximum power consumption. The low power modes are used to decrease the power consumption with a penalty on the output power. For the LP1 mode the supply can be reduced to 1.35 V and for the LP2 mode the supply is reduced to 1.25 V. An Analog Test bus is included for important node sensing.

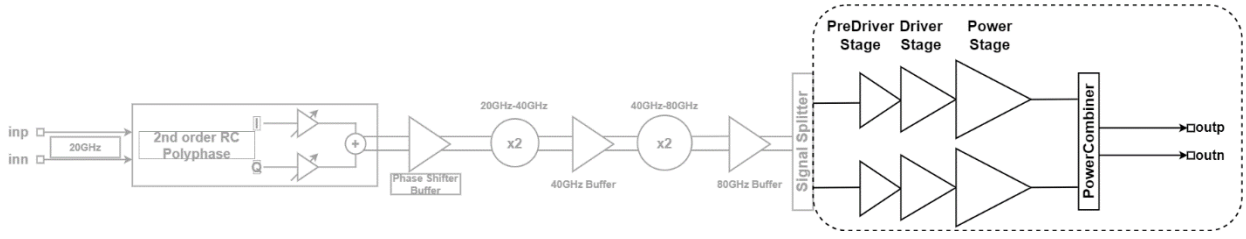
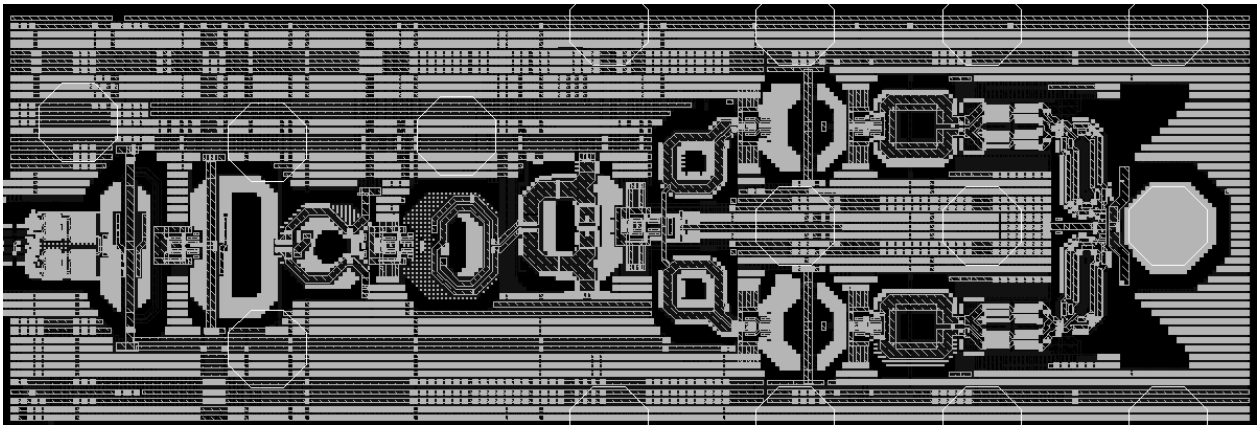


Figure 6. TX Power Amplifier Simplified Schematic

6. Register Summary

Register	Description	Nominal values
sl_atb_1hot<35:0>	Analog Test Bus	23
sl_dig_i<6:0>	Phase _select I	0
sl_dig_q<6:0>	Phase _select Q	0
sl_ibias_ctrl_da1<5:0>	bias current for Driver 1 Bias	57
sl_ibias_ctrl_da2<5:0>	bias current for Driver 2 Bias	57
sl_ibias_ctrl_dbl1<4:0>	BGR bias current for Doubler 1 Bias	8
sl_ibias_ctrl_dbl1_buf<2:0>	BGR bias current for Buffer 1 (after Doubler 1) Bias	2
sl_ibias_ctrl_dbl2<4:0>	BGR bias current for Doubler 2 Bias	13
sl_ibias_ctrl_dbl2_buf<2:0>	BGR bias current for Buffer 2 (after Doubler 2) Bias	2
sl_ibias_ctrl_pa1<5:0>	bias current for _pa 1 Bias	57
sl_ibias_ctrl_pa2<5:0>	bias current for _pa 2 Bias	57
sl_ibias_ctrl_pre_da1<5:0>	bias current for PreDriver 1 Bias	57
sl_ibias_ctrl_pre_da2<5:0>	bias current for PreDriver 2 Bias	57
sl_ibias_ctrl_ps<2:0>	BGR bias current for Power sensor Bias	3
sl_ibias_ctrl_ps_buf<2:0>	BGR bias current for Power sensor Buffer Bias	2
sl_pd_fast_da1	fast power down for Driver 1	0
sl_pd_fast_da2	fast power down for Driver 2	0
sl_pd_fast_dbl1	fast power down for Doubler 1	0
sl_pd_fast_dbl1_buf	fast power down for Buffer 1 (after Buffer 1)	0
sl_pd_fast_dbl2	fast power down for Doubler 2	0
sl_pd_fast_dbl2_buf	fast power down for Buffer 2 (after Buffer 2)	0
sl_pd_fast_pa1	fast pwer down for pa 1	0
sl_pd_fast_pa2	fast pwer down for pa 2	0
sl_pd_fast_pre_da1	fast power down for PreDriver 1	0
sl_pd_fast_pre_da2	fast power down for PreDriver 2	0
sl_pd_fast_ps	fast power down for Power sensor	0
sl_pd_fast_ps_buf	fast power down for Power sensor Buffer	0
sl_pd_power_sense_input	slow power down for Tx _slice bias	0
sl_pd_power_sense_out	slow power down for Tx _slice bias	0
sl_pd_slow_da1	slow power down for Driver 1	0
sl_pd_slow_da2	slow power down for Driver 2	0
sl_pd_slow_dbl1	slow power down for Doubler 1	0
sl_pd_slow_dbl1_buf	slow power down for Buffer 1 (after Buffer 1)	0
sl_pd_slow_dbl2	slow power down for Doubler 2	0
sl_pd_slow_dbl2_buf	slow power down for Buffer 2 (after Buffer 2)	0
sl_pd_slow_pa1	slow power down for _pa 1	0
sl_pd_slow_pa2	slow power down for _pa 2	0
sl_pd_slow_pre_da1	slow power down for PreDriver 1	0
sl_pd_slow_pre_da2	slow power down for PreDriver 2	0
sl_pd_slow_ps	slow power down for Power _sensor	0

sl_pd_slow_ps_buf	slow power down for Power _sensor Buffer	0
sl_pd_tx_slice_bias	slow power down for Tx _slice bias	0
sl_sw_i<1:0>	Quadrant _selector Ip	2
sl_sw_q<1:0>	Quadrant _selector Qp	2



Floorplan of the WEA7681TX22G

7. Availability

22FDX FD-SOI

8. Deliverables

GDSII, SystemVerilog Models

About weasic

weasic Microelectronics S.A. designs, develops, and markets high quality complex analog and RF IP for wireless communications and wireless sensors applications, helping semiconductor and system companies to shrink the product design cycle. WEASIC, silicon verified IP is designed in the state of the art CMOS, CMOS-SOI and SiGe processes and can be easily ported and customized to serve the development of 5G and Backhaul communications transceivers, mmWave front-end modules, and RADAR sensors.

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