76 GHz to 81 GHz FMCW Radar Receiver

1. Features

RF Input Frequency Range: 76 GHz to 81 GHz
LO Input Frequency Range: 38 GHz to 40.5GHz
Output Frequency Range: DC-120 MHz
Power Supply Voltages: 1.8V Analog, 0.8V RF, 0.8V Logic.
RX noise figure: 8.7 dB typ. (Includes 1dB loss from package to silicon transition)
Programmable RX Gain: 22.5 – 62.5 dB
RX In-band OIP3: 29 dBm
Input 1dBCP: -19 dBm (front end compression)
RX Channel Flatness @ 1GHz BW: 0.19 dB
Programmable IF Bandwidth:
Low Pass Filter Cut-off: 60 MHz - 120 MHz
High Pass Filter Cut-off: 2 MHz - 30 MHz
Automotive Grade 1 (-40 °C to 125 °C).
Power Consumption: 203 mW
Area:1450 um x 450 um

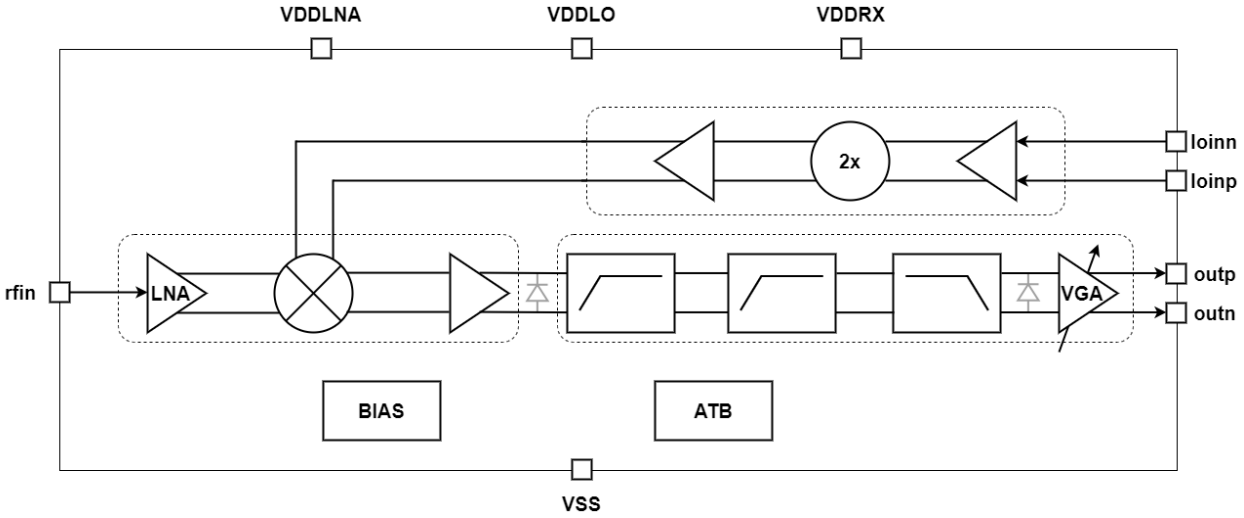
2. Applications

RADAR

3. Description

The WEA7681RX22G is a complete Zero-IF receiver for radar applications covering the 76 GHz to 81 GHz automotive band. The receiver integrates a Low Noise Amplifier, a down conversion mixer, a 1st order active highpass filter, a 1st order passive high pass filter and a 3rd order lowpass filter and a variable gain amplifier with digital gain control. The local oscillator chain is also integrated on the same IP. The LO accepts an input at 38 GHz to 40.5 GHz. The receiver has a dual saturation detector scheme for strong blocker detection at the mixer and the filter output. The receiver has a build-in Analog Test Bus (ATB) for complete monitoring of the bias conditions of all blocks, for FuSa. It is implemented in 22FDX FD-SOI process. The WEA7681RX22G occupies a silicon area of 1450 um x 450 um.

Simplified Schematic



4. Receiver performance

Feature		Conditions	Min	Typical	Max	Units
RF Input Frequency Range			76.0		81.0	GHz
LO Input Frequency Range			38.0		40.5	GHz
Output Common Mode			1.050	1.159	1.239	V
RX Max Gain		Including the losses of package to silicon transition (1dB typ. 1.5dB max.)	57.87	62.60	66.20	dB
Noise Figure	@50KHz	Including the losses of package to silicon transition (1dB typ. 1.5dB max.)		43.95	48.38	dB
	@300KHz			22.08	26.48	dB
	@1MHz			11.6	15.07	dB
	@3MHz			9.09	11.54	dB
	@50MHz			8.66	10.92	dB
RX Min Gain		Including the losses of package to silicon transition (1dB typ. 1.5dB max.)	18.32	22.56	25.10	dB
IF Pass-band ripple			-0.17		0.79	dB
Linear baseband full scale - differential		FS of the ADC – 3dB		400.0		mV
Gain Control Steps Resolution			1.64	2.52	3.01	dB
Gain drift over temperature					3.11	dB/55c
Input Return Loss					-6.43	dB
RF Chain Gain Flatness		Over a 1GHz BW		0.19	0.64	dB
Total RX power consumption		RX Chain : 97.2mW, Slice LO : 63.4mW, LO Dist : 183.9mW/8=22.98mW Common LO : 320.3mW/16=20mW			203.6	mW
Rx power-up time				58		us
RX Power Consumption		Power dissipation from three supplies: 0.8V for LNA, 0.8V for LO and 1.8V for Baseband and Bias			165	mW
HPF Cut-off Frequency - 3dB		For 30MHz -> 27.3MHz (9% error)	2.0	7.5	30	MHz
HPF Tuning Step Accuracy <30 MHz		Worst case at 27.5 MHz		10.5		%
HPF Tuning Step Accuracy at 30 MHz				46		%
LPF Cut-off Frequency - 3dB		145.3 MHz max overall cutoff	60.0	90.0	120.0	MHz
LPF Tuning Step Accuracy		After R/C Calibration		6.91		%
Absolute HPF cut-off freq - active		Worst case at 20MHz cutoff. 7.1% at 7.5MHz		9.70		%
LPF rejection at 350MHz			30.94	37.85		dB
Absolute HPF cut-off freq - passive (BPF)		Worst case at 30MHz cutoff 46.6% (44MHz max simulated HPF). All the other HPF cutoff have error less		10.5		%

	than 10.5%. At 7.5MHz the error is 6.1%				
Absolute HPF cut-off freq at 2MHz				3	%
Absolute HPF cut-off freq at 27MHz				14.88	%
RX Input 1dB Compression	With a low frequency blocker and 1st order high pass filter	-21.42	-18.33		dBm
RX IM2	Two tones: a low frequency blocker, and an in-band tone. RX max gain with 1st order high pass filter	62.63			dBc
RX IM3	Two tones: a low frequency blocker, and an in-band tone. RX max gain with 1st order high pass filter	59.93			dBc
RX In-band OIP3	IF chain P-out=0dBm and 2 in band tones	28.95			dBm
LO-leakage	Measured at the mmWave Receiver input		107.0		dB
ADC IF / LO spurs leakage @40GHz		-90			dBc
Offset error at ADC input	Monte Carlo simulation. FPVT Corner Simulation show 0.33mV offset			35.44	mV

5. Feature Description

5.1. Low Noise Amplifier

The low noise amplifier, a two-stage common source amplifier, provides high gain and increased isolation from the local oscillator. The single ended input is converted to differential with an integrated balun optimized for optimum noise and input matching simultaneously. The two-stage LNA has a total power gain of 14.5 dB, a typical noise figure (at 85°C) of 4.3 dB and a power consumption of 36 mW from 0.8 V supply.

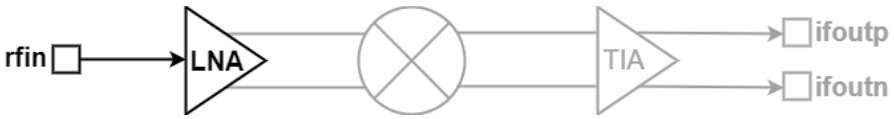


Figure1. Receiver Front End simplified schematic – LNA

5.2. Passive Mixer

The down-conversion is performed with a passive balanced mixer. The passive mixer has a conversion gain of -4 dB, typical noise figure (at 85°C) of 4 dB (7dB when accounting for the image noise folding) and zero power consumption.

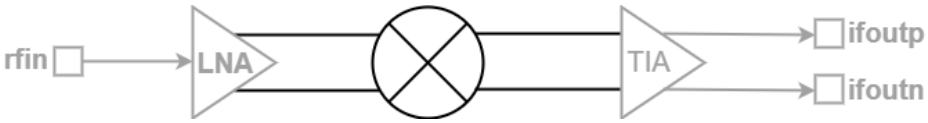


Figure2. Receiver Front End simplified schematic – Mixer

5.3. Transimpedance Amplifier

A TIA stage with programmable gain is connected to the output of the mixer. The equivalent power gain on the nominal gain setting is 23 dB, typical noise figure (at 85°C) is 4 dB with 16 mW power consumption from 1.8 V supply.

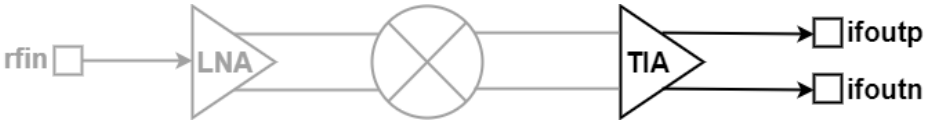


Figure3. Receiver Front End simplified schematic – TIA

5.4. High Pass Filter

The active High Pass filter is the first filter in the signal path, and filters out the low-frequency blockers. The design is a first order active high pass filter with gain. The cutoff frequency is programmable from 2 MHz to 30 MHz. The high pass section can be bypassed and then the block

operates as a gain stage. The filter has the ability to fine tune the cutoff frequency to minimize process variation effect to +/-10%. The gain control range is 21 dB with steps of 2.5 dB. The maximum gain of the block is 15 dB with a power consumption of 5.4 mW from 1.8V supply.

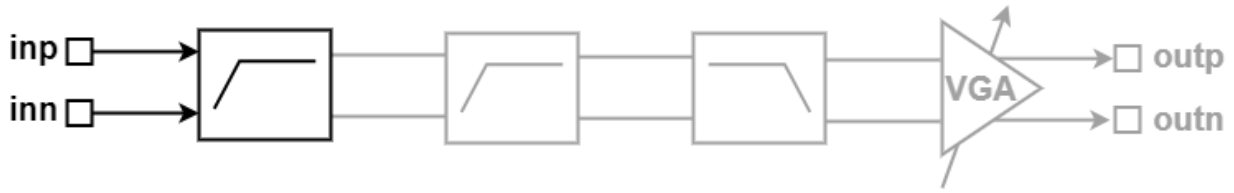


Figure4. Band Pass Filter simplified schematic – High Pass Filter

5.4. Band Pass Filter (High Pass + Low Pass filters)

The Band Pass filter is the second filter stage in the signal path. It consists of a passive first order high pass filter and a third order active low pass filter with Chebyshev response. The high-pass cutoff frequency is programmable from 2 MHz to 30 MHz and it is used to further attenuate low frequency blockers. The high-pass cutoff frequency is programmable from 60 MHz to 120 MHz with a bypass option which increases the filter BW to 145 MHz. The filter has a 0.8 dB passband ripple and the rejection at 350MHz is 31dB. This block also includes calibration capability to fine tune the cutoff frequency over process variation for both the high pass and low pass filters. The gain of the block is 0 dB with a power consumption of 16 mW from 1.8V supply.

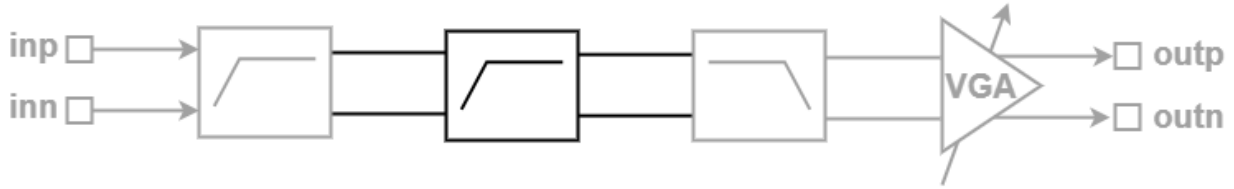


Figure5. Band Pass Filter simplified schematic – High Pass Filter

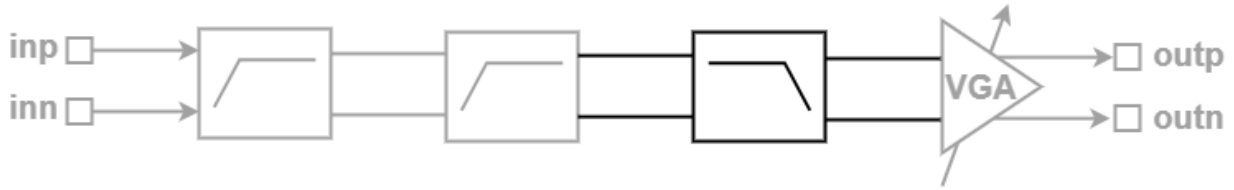


Figure6. Band Pass Filter simplified schematic – Low Pass Filter

5.5. Variable Gain Amplifier

The Variable Gain Amplifier is the last block in the receiver chain used to condition the signal for the ADC converter. The gain control range of the amplifier is 21dB with steps of 2.5 dB. The maximum gain of the block is 15dB with a power consumption of 5.76 mW from 1.8 V supply.

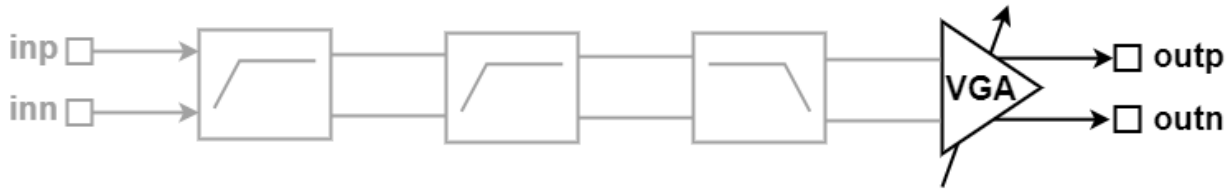


Figure7. VGA stage

5.6. Local Oscillator

The LO path consists of a 40 GHz buffer, a Doubler and a Mixer Driver. Both the input and output of the LO chain are differential signals. The passive mixer requires high input swing in the LO port to maintain good performance so in order to maintain reliability and performance over process variation, a power detector is connected to the output of the LO chain to calibrate the signal swing on the mixer input. The output of the detector is connected to an ADC and a digital FSM changes the bias conditions of the amplifiers till the predefined criteria are met. The ADC and digital FSM which are not a part of the WEA7681RX22G, can be supplied separately. The LO chain is powered from a 0.8V supply and the total consumption is 63 mW.

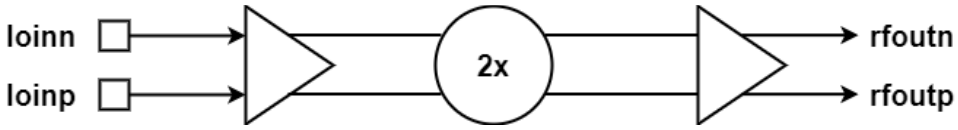


Figure8. LO path simplified schematic

6. Register Description

Field	Description
sl_bpfgainctrl	Filter Gain Control
sl_gainctrl1	Gain Control 1
sl_gainctrl2	Gain Control 2
sl_hpf1bypass	HPF 1st Pole Bypass
sl_hpf1prog	HPF 1st Pole Control
sl_hpf2bypass	HPF 2nd Pole Bypass
sl_hpf2prog	HPF 2nd Pole Control
sl_hpfrestrim	HPF Resistor Trim
sl_ibiasctrlbpf1	bias current Control for Bandpass filter
sl_ibiasctrldbl0_buf_lo	bias current Control for LO Buffer 1
sl_ibiasctrldbl1_buf_lo	bias current Control for LO Buffer 2
sl_ibiasctrldbl2_lo	bias current Control for LO Doubler
sl_ibiasctrlhpf1	bias current Control for HPF1
sl_ibiasctrllna1st	bias current Control for LNA1
sl_ibiasctrllna2nd	bias current Control for LNA2
sl_ibiasctrltiastage1	bias current Control for TIA Stage 1
sl_ibiasctrltiastage2	bias current Control for TIA Stage 2
sl_ibiasctrlvga	bias current Control for VGA
sl_ibiasoffsetlna1st	current offset Control for LNA1
sl_ibiasoffsetlna2nd	current offset Control for LNA2
sl_ibiasslopelna1st	current slope Control for LNA1
sl_ibiasslopelna2nd	current slope Control for LNA2
sl_lpfprog	LPF freq control
sl_pdbias_lo	Slice LO Bias Power Down
sl_pdbpf1	BPF 1st stage power down
sl_pdbpf2	BPF 2nd stage power down
sl_pdbpf3	BPF 3rd stage power down 1
sl_pdfastdbl0_buf_lo	Slice LO buffer 1 fast power down
sl_pdfastdbl1_buf_lo	Slice LO buffer 2 fast power down
sl_pdfastdbl2_lo	Slice LO doubler power down
sl_pdfetia	TIA Power down
sl_pdhpf1	HPF1 Power down
sl_pdlna1	fast power down for LNA 1st stage (RX _SLICE)
sl_pdlna2	fast power down for LNA 2nd stage (RX _SLICE)
sl_pdsatdet1	power Down of saturation detector 1
sl_pdsatdet2	power Down of saturation detector 2
sl_pdslowdbl0_buf_lo	Slice LO buffer 1 slow power down
sl_pdslowdbl1_buf_lo	Slice LO buffer 2 slow power down
sl_pdslowdbl2_lo	Slice LO doubler slow power down
sl_pdvga	VGA power down

sl_rxslicebiaspd	Slice Bias power down
sl_selcm	Slice common mode control 1
sl_selres	Slice common mode control 2
sl_spare	Spare common bits per slice
sl_tiagaincontrol	Slice TIA Gain Control
sl_atb1hot	Slice ATB bus
sl_pdpowerdet_lo	Slice LO detector power down
sl_filtertestmode_a	DDS A Channel enable
sl_filtertestmode_b	DDS B Channel enable
sl_lna1_bg_sel	LNA stage 1 Backgate control
sl_lna2_bg_sel	LNA stage 2 Backgate control

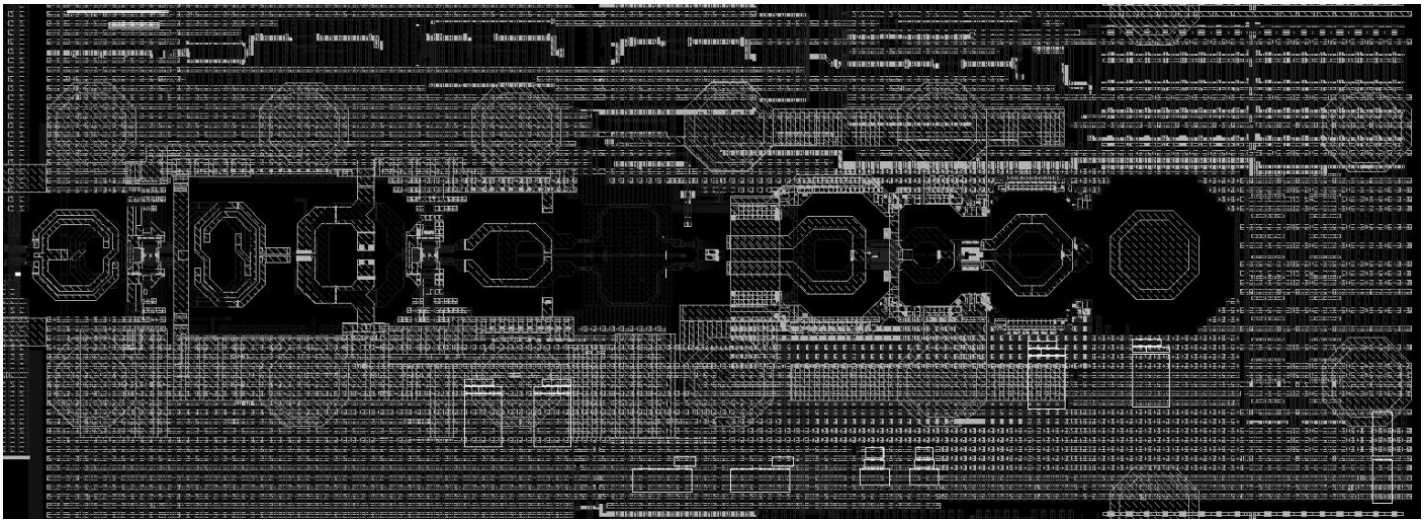


Figure9. Floorplan of the WEA7681RX22G

7. Availability

22FDX FD-SOI

8. Deliverables

GDSII, System-Verilog Functional models

About weasic

weasic Microelectronics S.A. designs, develops, and markets high quality complex analog and RF IP for the wired and the wireless communications industries, helping semiconductor and system companies to shrink the product design cycle. Weasic, silicon verified, IP is designed in the state-of-the-art CMOS and SiGe processes and can be easily ported and customized to serve the development of transceivers for 5G communications, Mobile Backhaul, RADAR sensors and 802.11.* applications.

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